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**In the claims**

1.(currently amended) A multimode clock recovery circuit for ~~providing~~ use in the provision of constant bit rate services in a cell relay network, comprising:

~~an embedded~~ digital phase locked loop including a digital controlled oscillator for generating an output signal, a loop filter responsive to a phase signal to control said digital controlled oscillator, and a phase detector having multiple inputs for receiving different types of input signal;

said phase detector comparing an input signal applied to any of said multiple inputs with said output signal to develop said phase signal;

~~including an input circuit capable of generating a phase signal from at least two types of input signal, said phase signal controlling the output of said phase locked loop to generate clock signals for said constant bit rate services~~a local SRTS generator for generating time stamps from said output signal connected to one of said multiple inputs of said phase detector;

said phase detector in SRTS mode developing said phase signal from said locally generated time stamps and time stamps received over said cell relay network;

another of said multiple inputs of said phase detector being adapted to receive a line rate clock signal;

said phase detector in line rate mode developing said phase signal from said line rate clock signal and said output signal; and

a receive buffer for receiving incoming cells that in an adaptive mode develops said phase signal from a state of said buffer and applies said phase signal developed by said receive buffer to said loop filter to control said digital controlled oscillator.~~,~~

2.(currently amended) A multimode clock recovery circuit as claimed in claim 1, wherein said ~~input circuit is adapted to receive~~receive buffer develops said phase signal in the form of ~~a~~ phaseword ~~from a receive buffer for incoming cells to permit clock adaptive recovery~~ based on the fill level ~~of the receive buffer for incoming cells~~thereof.

3.( currently amended) A multimode clock recovery circuit as claimed in claim 2, wherein said phaseword is derived from the write_pointer – read_pointer – *average* of said receive buffer, where *average* is a parameter set by the user.

4.(cancelled)

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5.(currently amended) A multimode clock recovery circuit as claimed in claim 41, wherein said phase detector comprises a common up/down counter for developing said phase signal in said SRTS and line rate modes.

6.(currently amended) A multimode clock recovery circuit as claimed in claim 5, whercin ~~the~~ an output of said common up/down counter ~~does not wrap around and the output of the common up/down counter~~ is fed to an accumulator ~~to track the output of the up/down counter without applying a modulo function~~.

7.(currently amended) A multimode clock recovery circuit as claimed in claim 6, ~~wherein~~ comprising a shifter for adjusting the weight of the output of said common up/down counter.~~the weighted output is fed to the accumulator.~~

8.(currently amended) A multimode clock recovery circuit as claimed in claim ~~6~~7, wherein said shifter adjusts the weight of said ~~the weighted output of the~~ up/down ~~counter can be changed for receiving either~~according to whether said recovery circuit is in SRTS mode or line rate mode ~~a clock signal or a signal from a timestamp circuit~~.

9.(currently amended) A multimode clock recovery circuit as claimed in claim 8, wherein said shifter sets the weight of said up/down counter ~~is programmable~~ to sixteen for a timestamp signal and one for a clock signal.

10.( currently amended) A multimode clock recovery circuit as claimed in claim ~~8~~1, wherein said phase detector comprises ~~further comprising~~ first and second difference circuits, each receiving at first and second inputs thereof current time stamps and delayed time stamps, said first difference circuit receiving time stamps from said cell relay network and said second difference circuit receiving time stamps generated by said local SRTS generator, ~~each receiving an SRTS input signal and an SRTS input signal delayed by one cell, the first circuit receiving its SRTS form the network, and the second difference circuit receiving its SRTS signal from a local SRTS generator, the~~said first and second difference ~~differenee~~ circuits providing ~~an~~ respective inputs to ~~said~~ an up/down counter, a subtractor having inputs for respectively receiving time stamps received over said cell relay network and time stamps generated by said local SRTS generator, and an ~~and the second difference circuit providing an input to a subtractor, the output of said difference circuit being fed to said accumulator with the weighted output of said up/down~~

~~counter~~accumulator for receiving the outputs of said subtractor and said up/down counter, to develop said phase signal.

11.(currently amended) ~~11.~~ A multimode clock recovery circuit as claimed in claim ~~5~~10, ~~further comprising a local synchronous residual timestamp (SRTS) generator in the feedback loop of the phase locked loop~~wherein the output of said up/down counter is weighted.

12.(original) A multimode clock recovery circuit as claimed in claim ~~11~~1, wherein said ~~said local SRTS generator~~ local SRTS generator comprises a divider for receiving a feedback signal from the output of the phase locked loop, a counter for receiving ~~the~~ a network clock signal, and a register for generating ~~a~~ local SRTS ~~signal~~time stamps.

13.(currently amended) A multimode clock recovery circuit as claimed in claim 11, wherein said ~~the~~ up/down ~~inputs of the counter receive the respective network clock signal and the local SRTS signal~~counter is a non wrap around counter.

14.(original) A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into holdover mold wherein the output of the phase locked loop remains constant when a valid input signal is lost so as to maintain a constant frequency based on the last valid input signal.

15.(original) A multimode clock recovery circuit as claimed in claim 1, wherein the phase locked loop goes into holdover mode when any of the following conditions occur: receive buffer runs out of SRTS values in the SRTS mode, a virtual circuit through said network times out, and loss of synchronization is asserted in a line rate mode.

16.(cancelled)

17.(cancelled)

18.( currently amended) A multimode clock recovery circuit for use in providing constant bit rate services in a cell relay network, comprising a phase detector having multiple inputs, a loop filter receiving the output of said phase detector, a digital controlled oscillator receiving the output of said loop filter, a jitter reduction circuit receiving the output of said digital controlled oscillator, a divider receiving the output of said jitter reduction circuit, and ~~an~~ local SRTS generator in ~~the~~ a feedback loop ~~of said digital controlled oscillator~~connected to one of said multiple inputs of said phase detector, said local SRTS generator generating local time stamps

derived from the output of said digital controlled oscillator, and said phase detector developing a phase signal for controlling said digital controlled oscillator from said local time stamps and time stamps received from said cell relay network, and wherein said local SRTS generator includes a wrap-around counter, said phase signal is developed from the difference between the time stamps received from said local SRTS generator and said time stamps received over said cell relay network, and said phase detector includes a weighted non-wrap around up/down counter that is added to said difference.

19.( currently amended) A phase detector for recovering clock signals from received time stamps in a cell relay network providing constant bit rate services, comprising a first input for receiving a remote time stamp signal, a second input for receiving a locally generated time stamp signal, comparators for comparing the current time stamps with the previous time stamps to generate ~~a carry signal~~, a weighted non-wrap around up/down counter receiving the ~~inputs~~ outputs of said respective comparators, a subtractor for deriving the difference ~~of~~ between said remote time stamp and said locally generated time stamps, and an accumulator for adding the output of said subtractor to the output of said weighted non-wrap around up/down counter to generate a phase output signal for controlling a digital controlled oscillator.

20.( currently amended) A phase detector as claimed in claim ~~18~~ 19 having an error input for receiving an error flag ~~to disable the counter when an error occurs~~.

21.( currently amended) A phase detector as claimed in claim 19, further comprising a register connected to the output of said ~~adder~~ accumulator for temporarily storing the phase output.

22.( cancelled)

23.( cancelled)

24.(cancelled)